A Comparative Analysis of Ring Oscillator Configurations Utilizing CMOS Inverters and Differential Pair Amplifiers as Delay Elements

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***Abstract*—Ring oscillators are essential blocks for integrated circuits, acting as digital clock generators. There are several implementations techniques for this oscillator. However, the choice of the most adequate topology of ring oscillator demands the analysis of the trade-offs with respect to electrical characteristics. This paper presents a comparative study between two topologies for the implementation of a ring oscillator. Each topology uses a specific delay cell: a CMOS inverter or a differential pair amplifier. The target output frequency is 10.44 MHz and the oscillators were implemented in 130 nm technology. The topologies are compared in terms of power dissipation, silicon area and manufacturing process variation. Electrical simulations show that the inverter ring oscillator presents a smaller power consumption and a smaller silicon area. By the other side, the differential amplifier oscillator presents a smaller sensitivity to process variation. These results can help to guide the designer to decide the best topology that fits the system requirements in an integrated circuit design.**

***Index Terms*—Inverter, differential pair, ring oscillator, manufacturing process variation.**

I. Introduction

Ring oscillators (ROs) are essential building blocks in the construction of integrated circuits. They have the function of acting as digital clock generators, which is extremely important for electronics. With the development of methods for the application of ring oscillators, different topologies have proven useful for specific applications, with advantages in some parameters and disadvantages in others. Power dissipation and temperature variations are the main concerns for any oscillator application [1].

In the CMOS (Complementary Metal-Oxide-Semiconductor) process, logic gates can not change the logic level instantaneously, because its parasitic capacitance must be charged (or discharged). As a consequence, the output of each stage of an oscillator changes after a certain delay time. In general, the more stages an oscillator has, the higher the propagation delay, and therefore, the lower the oscillation frequency. This is because the delay of each stage accumulates, reducing the oscillation rate. It is important to note that, in addition to the number of stages, other factors such as the resistance and capacitance of individual components can also affect the oscillation frequency of the circuit [2] [3].

In general, a simple ring oscillator has several delay stages connected in series to generate gain so that a loop is obtained at the output, usually in the form of voltage [4].

The oscillation frequency F_o of a simple RO is determined by the expression in eq. 1, where N refers to the number of stages, C_{tot} correponds to the total output capacitance of each stage (parasitic capacitances of the devices and the load capacitance), I_d is the transistor drain current that is common for all stages and V_{dd} is the supply voltage of the circuit. Thus, the greater the value of N, the greater the signal delay time [5]. Therefore, it is possible to change the oscillation frequency of a simple RO by varying the number of stages [6].

$$F_o = \frac{I_d}{NC_{tot}V_{dd}} \tag{1}$$

The goal of this work is to analyze two distinct topologies for the implementation of a ring oscillator: using CMOS inverters and using differential pair amplifiers as delay cells. Subsequently, an analysis of the results obtained through simulations will be carried out to compare which of the two topologies proved to be more efficient. It is important to highlight that the technology used in this work is an 130 nm CMOS process with V_{DD} of 1.5 V.

The remaining of this work is organized as follows: in section 2, a brief description of the ROs is presented, as well as the analysis of the used methodology and, thus, the two models studied; in section 3, the obtained results are discussed, including a comparison between each RO topology; Section 4 is devoted to presenting the conclusion of the study, as well as comments on the direction for future analysis.

II. Ring Oscillator Topologies

A. CMOS Inverter Ring Oscillator

The CMOS Inverter Ring Oscillator is one of the most popular architectures for the design of ROs due to the simplicity of implementation, using only CMOS inverters. The parameters of this architecture were chosen in this work to achieve an

oscillation frequency equivalent to 10.44 MHz. The values of the parameters used in the design of each CMOS inverter are shown in the Tab. I. A total of five stages of inverters were used, as shown in Fig. 2, to generate the necessary delay and achieve the desired oscillation frequency. It is worth mentioning that the value of the channel width (W) of the PMOS transistor in the inverters is about 3.9 times greater than the W of the NMOS transistor, in order to compensate the low mobility of holes and equalize high-to-low and low-to-high delay times [7].

To estimate the dynamic power comsuption of the CMOS Inverter Oscillator, one of the methods is to integrate the drain current of the PMOS inverter along a given period, as shown in eq. 2:

$$P = N \cdot \frac{1}{T} \int_0^T I_d.V_{dd}\ dt, \tag{2}$$

where I_d corresponds to the drain current of the PMOS transistor belonging to the inverter architecture, and T corresponds to the period in which the integral calculation will be performed. By integrating the current the dissipated energy is obtained. Simply dividing this energy by the period T we obtain the dynamic dissipated power. The resulting value is multiplied by the number of stages. As the stages are connected in series, they end up having the same current coming from the supply voltage V_{DD} entering the PMOS transistor's drain terminal. The designed RO dissipated a total dynamic power equivalent to $23.5780\ \mu W$ to achieve the desired oscillation frequency. This value can be considered the total dissipated power, since the static power dissipation of a CMOS inverter is close to zero.

One of the analyzes that must always be taken into consideration is regarding the total area of the oscillator, since in modern processes we always want to occupy the smallest possible area in order to be able to assign more circuits on the same chip. The estimated total gate area for this designed architecture is $1.6593\ \mu\text{m}^2$.

Process variations are inherent to any manufacturing process, and therefore differences in parameters can show up in noticeable or subtle ways. To try to predict these differences, a Monte Carlo simulation is performed, in which a selected number of rounds vary the parameters that normally suffer the effect of the manufacturing process. In order to show how the inverter oscillator behaves with respect to manufacturing processes, a simulation with 500 runs was performed. Figure 4a shows how the oscillation frequency is affected by variations induced by the manufacturing process, with a standard deviation (σ) of 554.089 kHz, and an average (μ) of F_o = 10.42 MHz.

TABLE I: Design parameters for the inverter oscillator

Parameter	Value
L (NMOS)	$225\ nm$
L (PMOS)	$225\ nm$
W (NMOS)	$300\ nm$
W (PMOS)	$1.175\ \mu m$
V_{DD}	$1.5\ V$
N (Stages)	5

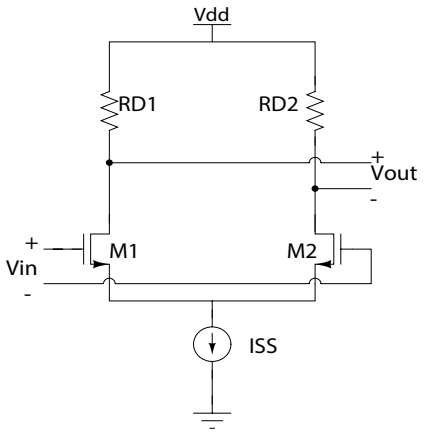


Fig. 1: Schematic of the differential pair.

B. Differential Pair Amplifier Ring Oscillator

The ring oscillator implemented with differential pair amplifiers is another architectural topology that can be implemented for an RO. This topology uses the differential pair as a delay cell to generate the oscillation, instead of the inverters.

In general, the basic differential pair is composed of two matched input transistors, that have the same W/L ratio. Their sources are biased by a reference current source I_{ss} and there are two resistors R_d of the same value connected to the drain of each transistor to generate the desired amplifier gain, as shown in Fig. 1 [8].

Similar to the inverter, the number of oscillation stages affects the oscillation frequency of the RO. Mathematically, the equation to calculate F_o follows a similar form to eq. 1. The difference is that, instead of considering just capacitance loads, there are also resistances R_{tot} of the differential pair to be considered, as shown in eq. 3:

$$F_o = \frac{I_d}{NC_{tot}R_{tot}V_{dd}} \tag{3}$$

To design the architecture of the amplifier oscillator, it is first necessary to define that the amplifier to be designed must have a gain of 10 V/V with a reference current $I_{ss} = 5.5\ uA$, in order to operate in the region of moderate inversion of the transistors. Using the equation for the gain of an amplifier shown in eq. 4, the value of the transconductance gm and resistances R_d were determined to reach the desired gain [8] [9].

$$A_d = -g_m R_d \tag{4}$$

Table II shows the sized design parameters for the differential pair amplifier.

To reach the desired frequency of 10.44 MHz, 4 amplifiers were placed in series, as shown in Fig. 3. In the third amplifier, the positive differential output connects to the negative

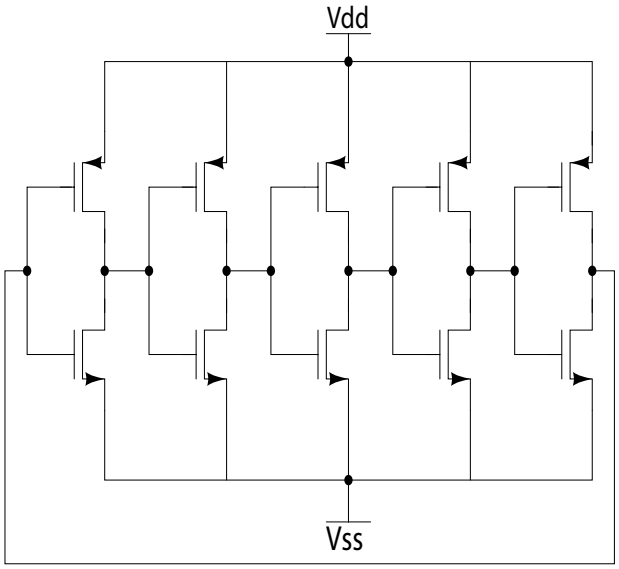


Fig. 2: Schematic of the 5-stage inverter ring oscillator.

differential input of the next stage, in order to generate the oscillation of the RO [10]. The calculation of the dissipated power is carried out in a simple way, multiplying the reference current I_{ss} by the V_{dd} supply voltage, thus obtaining the dissipated power per stage. Then, multiplying by the number of stages, the total power dissipated is obtained, as shown in eq. 5:

$$P = (I_{ss}.V_{dd})N \tag{5}$$

The total static power for this oscillator topology is equivalent to 33 μW, proving to be a considerable power, since we are using resistors to obtain the gain in this amplifier topology.

The analysis in terms of area was done in the same way as for the inverting oscillator. The differential pair RO architecture occupies a gate area of approximately 111.74 μm^2.

The Monte Carlo simulation for the oscillator with differential pair was performed in the same way as for the RO inverter, using 500 simulation runs. The simulation showed that, regarding variation in the manufacturing processes, this topology obtained a smaller variation with respect to the output oscillation frequency, even considering the variation in the resistive elements. The histogram shown in Fig. 4a presents the simulation results with an average oscillation frequency of F_o = 10.55 MHz, which diverged by 0.11 MHz from the nominal frequency value at which the oscillator was designed, with a standard deviation of 455.187 kHz.

TABLE II: Differential amplifier design parameters

Parameter	Value
L (NMOS)	0.60 μm
W (NMOS)	18.37 μm
A_v	10 V/V
I_{ss}	5.5 μA
V_{dd}	1.5 V
R_d	300 kΩ

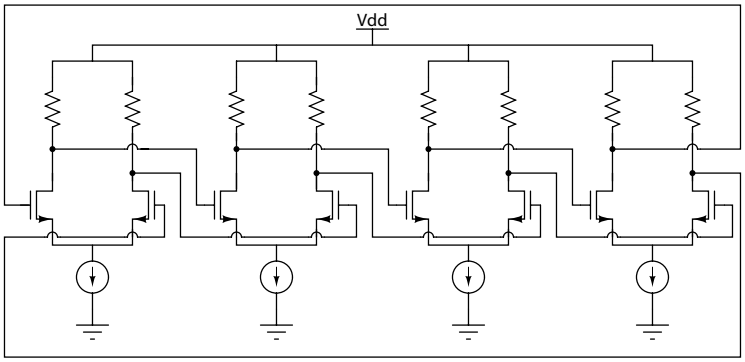
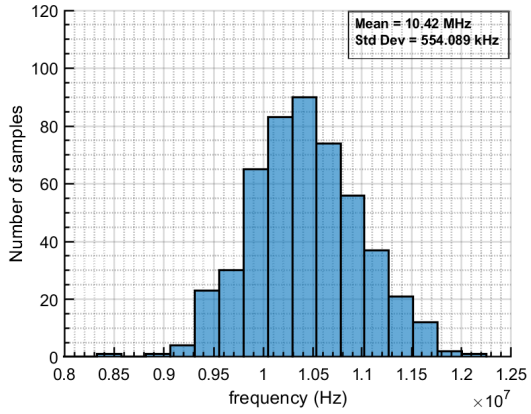
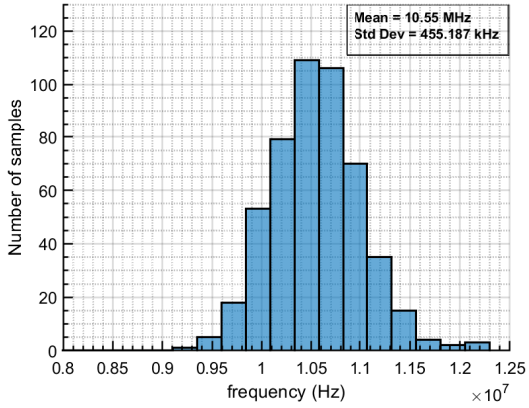


Fig. 3: Four-stage differential pair ring oscillator.



(a) Inverter oscillator.



(b) Differential pair oscillator.

Fig. 4: Simulation results for the 500-run Monte Carlo simulation of the oscillation frequency for the two studied oscillator topologies.

III. Comparison of the results obtained from each topology

As previously confirmed, the two models of oscillators presented in this work were able to reach the desired operating frequency of 10.44 MHz, with a maximum operating voltage of 1.5 V, thus generating an oscillaton signal as shown in the

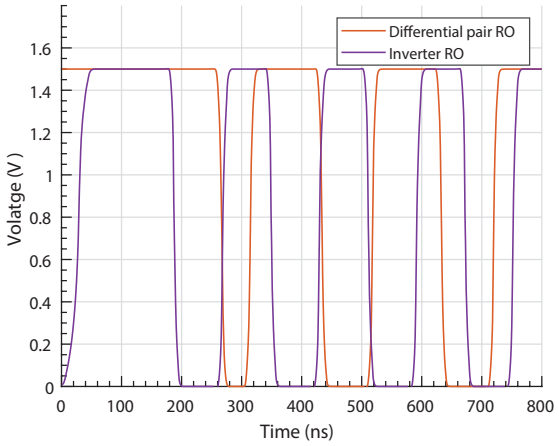


Fig. 5: Output voltage of the proposed oscillator models.

graph fig.5. It is worth noting that to obtain the waveform of fig.5, a simple buffer was placed at the output of the oscillators table.III. These buffers have high values of W to perform a quick operation on the output of the oscillator so that the value varies from 0 to V_{DD} as quickly as possible. We used the same output buffers for both implemented oscillator topologies.

The results referring to the power dissipation show that the CMOS inverter ring oscillator presented a power dissipation lower than the differential pair amplifier ring oscillator, due to the fact that the inverter RO does not present relevant static power dissipation. One of the solutions to make the power dissipation of the differential amplifier RO closer to that of the inverter RO would be to decrease the reference current I_{ss}. However, as shown by eq. 3, changing the current would also change the oscillation frequency. Furthermore, the resistances R_d of the differential pair would have to be increased to maintain the gain of $10\ V/V$ of the amplifier. In the manufacturing process, it is known that resistors are the elements that vary the most, which is also shown by the Monte Carlo simulation of the RO differential amplifier.

In any integrated circuit, area is an important factor, and the differential pair amplifier RO achieved a gate area considerably larger than the inverter RO.

Process variations are always present in any manufacturing process, and the Monte Carlo simulation of the inverter RO inverter showed a higher standard deviation for the RO, while maintaining an average in the target oscillation frequency. On the other hand, the simulations of the model with the differential pair showed a considerably smaller standard deviation for different manufacturing processes, which means that, in different samples, the results referring to the frequency will vary much less from the value which was designed. This low standard deviation shows that the resistive elements did not significantly affect circuit electrical characteristics, since, as previsously mentioned, they are the elements that vary most with the manufacturing process. Furthermore, the presented model uses an ideal reference current source, which does not further increase the standard deviation, as would be the case if an ideal current source using transistors were used.

TABLE III: Design parameters for the buffer

First stage of buffer	Second stage of buffer
W (NMOS) = 3.675 um	W (NMOS) = 11.025 um
L (NMOS) = 130 nm	L (NMOS) = 130 nm
W (PMOS) = 11.025 um	W (PMOS) = 33.075 um
L (PMOS) = 130 nm	L (PMOS) = 130 nm

IV. Conclusion

In this article, a comparison of two different topologies for the implementation of a ring oscillator in an CMOS 130 nm technology was approached. The first analysis was performed using 5 stages of CMOS inverters, while the second used 4 stages of differential pair amplifiers. The obtained results are relevant to make such a comparison, since the power dissipation refers to the losses in the circuit and the area corresponds to the cost. The inverter oscillator proved to be much more efficient if we consider the aspect related to the lower dissipated power, in addition to the ease of implementation, since it is completely based on MOS inverters. However, when considering process variation, it is possible to notice a considerably higher sensitivity in the RO inverter than in the RO differential pair. This can be critical when the oscillation frequency value must match a desired value.

However, a limitation of the study is that the differential amplifier oscillator was implemented using an ideal current source. Furthermore, it should be borne in mind that changes can still be made to the parameters used for this model. This will be the subject for future work, in order to improve the differential amplifier RO to perform the same comparisons made in this work and also to study how we can control the variation of the operating frequency for both topologies, implementing a VCO (voltage controlled oscillator).

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